



(2815/17)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 037267-0135

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SEP 14 2001
C-2800 MAIL ROOM

In re patent application of

Takaaki NAGAI et al.

Serial No.: 09/606,159

Group Art Unit: 2815

Filed: June 29, 2000

Examiner: Paul E. Brock II

For: EEPROM SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE
SAME

CERTIFICATE OF MAILING

Commissioner for Patents
Washington, D.C. 20231

Commissioner:

I hereby certify that the following paper(s) and/or fee along with any attachments referred to or identified as being attached or enclosed are being deposited with the United States Postal Service as First Class Mail under 37 C.F.R. § 1.8(a) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington D.C. 20231.

1. Information Disclosure Statement
2. PTO/SB/08B
3. Check No. 595978 (\$180) for fee
4. Postcard

Respectfully submitted,

September 7, 2001

Date

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INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.56 AND 37 CFR 1.97

Commissioner for Patents
Washington, D.C. 20231

Commissioner:

Submitted herewith on a modified Form PTO/SB/08B is a listing of document(s) known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 C.F.R. § 1.56. A copy of the listed document(s) is being submitted to comply with the provisions of 37 C.F.R. §§ 1.97-1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 C.F.R. § 1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* prior art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The instant Information Disclosure Statement is being filed after the mailing date of a final action but before the payment of the issue fee under the provisions of 37 C.F.R. § 1.97(d), and is accompanied by a statement specified in 37 C.F.R. § 1.97(e) and a fee set forth in 37 C.F.R. § 1.17(p).

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RELEVANCE OF EACH DOCUMENT

The document(s) listed on the attached PTO/SB/08B were cited as being relevant during the prosecution of the corresponding Japanese application. A copy of an English language abstract of the listed documents, if available, is being provided. The absence of a translation or an English-language counterpart document does not relieve the PTO from its duty to consider this document (37 C.F.R. § 1.98 and M.P.E.P. § 609).

The Examiner in the corresponding Japanese patent application has commented as follows:

Ref. No. 37267/135 SN: 09/606159

Note (For cited literature, etc., see List of Cited Literature)

Claim 1, 2, 3

Reason 1

Cited literature 1, 2, 3, 4

Remarks:

Described in Cited Literature 1 is the fact that a common source line is formed using a first layer of aluminum routing, and a bit line is formed using a second layer of routing, as well as the fact that a conductive layer 25 is formed in the drain region. (Specifically, refer to Cited Literature 1, Figure 4 and page 4, from the upper-right column, line 18 to the lower-left column, line 2.)

Described in Cited Literature 2 is the fact that a common source line is formed using a first layer of routing, and a bit line is formed using a second layer of aluminum routing, as well as the fact that a plug-shaped contact 209 is formed in the drain region. (Specifically, refer to Cited Literature 2, Figures 1 and 2, and the places where they are explained.)

Described in Cited Literature 3 is the fact that a common source line is formed using a first layer of routing, and a bit line is formed using a second layer of routing, as well as the fact that a pad 23 is formed in the drain region. (Specifically, refer to Cited Literature 3, Figures 2 and 7, and their explanation.)

Described in Cited Literature 4 is the fact that a common source line is formed using a first layer of aluminum routing, and a bit

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line is formed using a second layer of aluminum routing. (Specifically, refer to Cited Literature 4, Figure 1, and its explanation.)

Consequently, by referring to Cited Literature 4, a person skilled in the art could easily have conceived of using aluminum for the first layer of routing, and using aluminum for the second layer of routing for the inventions described in Cited Literature 1 through 3.

Furthermore, Cited Literature 4 describes the fact that a bit line may be formed using a first layer of aluminum routing, and a common source line may be formed using a second layer of aluminum routing (specifically, refer to Cited Literature 4, Figure 1 and page 2, from the upper-right column, line 18, to the lower-left column, line 2), therefore a person skilled in the art could easily make a first layer of aluminum routing into a bit line, and a second layer of aluminum routing into a common source line in Cited Literature 1 through 3.

Claim 4

Reason 2

Cited literature 1, 2, 3, 4, 5

Remarks:

Because forming non-volatile memory and CMOS logic circuit on a single substrate was common knowledge at the time of this application, (For example, refer to Cited Literature 5, Figure 5 and the place where it is explained.) the invention of Claim 4 of this application could easily have been conceived by a person skilled in the art.

Claim 5

Reason 2

Cited literature 1, 2, 3, 4, 6

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Remarks:

Because forming routing to back a word line in order to decrease the resistance of the word line was common knowledge at the time of this application (for example, refer to Cited Literature 6, Figure 1 and its explanation), the invention of Claim 5 of this application could easily have been conceived by a person skilled in the art.

List of Cited Literature

Japanese Unexamined Patent Publication H03-057281

Japanese Unexamined Patent Publication H07-074326

Japanese Unexamined Patent Publication H05-259475

Japanese Unexamined Patent Publication S56-100448

Japanese Unexamined Patent Publication H09-135008

Japanese Unexamined Patent Publication S63-211769

Record of Prior Art Literature Search Results

Searched Fields: IPC 7th Edition H01L 27/115

H01L 21/8247

H01L 29/788

H01L 29/792

Prior Art Literature

Japanese Unexamined Patent Publication H08-264737

Japanese Unexamined Patent Publication H09-082926

Japanese Unexamined Patent Publication H03-052267

Reference H05-259475 listed above is in the same family of patents as U.S. Patent No. 5,210,047 submitted herewith.

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Reference H08-264737 listed above is in the same family as U.S. Patent No. 5,741,719 submitted herewith.

This Record of Prior Art Literature Search Results does not constitute a reason for rejection.

FEE

A fee in the amount of \$180.00 in accordance with 37 CFR 1.17(p) is attached.

CERTIFICATION

The undersigned hereby certifies in accordance with 37 CFR 1.97(e)(1) that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to the filing of this Statement.

Respectfully submitted,

September 7, 2001

Date

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Should additional fees be necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge Deposit Account No. 19-0741 for any such fees; and applicant(s) hereby petition for any needed extension of time.